

# Transceiver Front-End Technology for Software Radio Implementation of Wideband Satellite Communication Systems

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## Keywords

Software Radio, Reconfigurable Payload, Transceiver Front-end, Wideband Receiver, Satellite Communication

## 1. Introduction

The term Software Radio (SR) is used to encompass a wide range of agile, multimode, programmable radio systems that can operate over a wide frequency band, and be able to “speak” the language of the different protocols (IEEE Com., 1995)-(IEEE Pers., 1999). The evolution in the semiconductor industry leading to constant increase in the clock speeds and increase in device density, and the advent of reconfigurable hardware have paved the way to the creation of SR platforms. SR uses a mix of hardware entities for the implementation of radio transceiver functions capable of commanding the Radio Frequency (RF) spectrum. This mix includes high-speed DSPs, multiple ASICs, parameterized hardware, switchable microcode, multiprocessor arrays (such as very long instruction word architectures), reconfigurable logic and a combination of any of the above.

The evolution of space systems whether for environmental monitoring, experimentation, deep space exploration or communication applications has been towards the creation of a reconfigurable and programmable platform that could leverage the initial investment costs of the satellite, by providing the flexibility that renders the satellite more useful and up-to-date with respect to the latest advances in the sciences. This flexibility allows for intelligent management of the payload with potentially multiple uses throughout the life of the satellite.

The future broadband integrated systems shall rely more on more on technological and networking solutions that allow interoperability of a

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host of devices in a heterogeneous terrestrial and space based networks with varying capabilities. The two key aspects of the future evolution of broadband integrated systems are a) multi-function terminals capable of interoperating among a variety of broadband access technologies and protocols (i.e., SR terminals) and b) novel networking paradigms and solutions build around the basic concepts of service personalization and smooth ubiquitous handoff between different types of systems all with a certain degree of transparency to the user and with high efficiency.

An important component of the space system is its transceiver which is responsible for all the communication functions between the satellite and the earth station. Current trends are towards the implementation of the satellite transceiver using the SR technology. The use of the SR technology is not just for the implementation of the satellite's communication payload, rather, there are ample reasons for interest in this technology for the implementation of the satellite's ground base-station transceiver as well. Indeed, from a commercial point of view, the truly programmable SR systems may find their first application in the space sector until eventually due to constant evolution in the semiconductor industry, they also find widespread use in terrestrial systems.

In addition to the SR technology, the use of smart antennas is envisioned in the design of the future satellite systems. The use of smart antennas can enhance the capacity (or range) of the RF link through a combination of diversity gain, multipath mitigation, and interference cancellation. This technology permits electronic steering of the radiation pattern providing great flexibility in comparison to the traditional antenna systems with mechanically steerable radiation pattern. The main application domain of this technology are: 1) satellite tracking, 2) direction of arrival estimation, 3) adaptive beam-forming, and 4) signal to interference plus noise ratio enhancement of the overall system.

In addition to these system level trends, there are strong motivations behind the use of Commercial Off The Shelf (COTS) and Commercial-Avionics-Military (CAM) components as the building blocks of the communication systems. This push comes from the need to enhance the signal processing capabilities of the satellite's payload which are currently limited due to the radiation tolerance requirements of space electronic systems.

The key advantages of such a design paradigm for future satellite communication systems are:

- low cost robust, reliable and reconfigurable system based on the use of COTS and CAM components;

- dynamic transceiver management based on the requirements of the application and its time evolution;
- transceiver performance improvement based on the incorporation of the latest algorithms and signal processing techniques;
- payload cost reduction and potential export of the system architecture in such areas as base station design for cellular telephony applications for revenue generation outside the space sector;
- real-time user access to transceiver functions for telescience applications;
- dynamic system modification with no down-time;
- well balanced high computational capacity transceiver architecture.

While there are many advantages to the use of SR technology for construction of reconfigurable satellite payloads, we should note that the latency plays a critical role in the design of the SR transceiver. This is because the satellite link by itself introduces large delays due to the great distances involved, putting even more stringent limits on the transceiver tolerable delays than in other applications. The issue of latency for SR transceiver should really be addressed at the hardware level via a proper partitioning of the transceiver functions among general purpose processors, reconfigurable logic such as FPGAs, embedded systems and DSP boards. In other words, certain architectural solutions for the SR hardware platform itself would have to be excluded simply on the basis of the end-to-end delay considerations.

Within this broad application domain of the SR technology to the satellite communication system design, this paper focuses on a key aspect of the design of a truly wideband SR system, namely, that of the system front-end and in particular, the wideband Analog to Digital Converter (ADC). With reconfigurable and multipurpose processor hardware abundant in the market place, the design of a low power truly wideband ADC still poses a serious technological challenge.

In this paper, we look at the front-end architecture of wideband receivers, outline the key aspects of the design of such front-end systems, specify the performance metrics associated with their design, present an architecture of a wideband ADC based on one of the most promising techniques that combines signal down conversion and sampling, that is, the Delta-Sigma modulator structure, and finally present the results of our design, implementation, and test campaign of a prototype

PC-based SR system employing a proprietary high-speed ADC from TechnoConcepts, Inc. (<http://www.technoconcepts.com>).

## 2. Broadband Front-Ends, an Overview

Third and fourth generation communication standards for terrestrial wireless and satellite applications employing broadband, multimode, multicarrier Software Radio systems require very high levels of performance from the system front-end and the Digital Signal Processing (DSP) units. The goal is to miniaturize the integrated circuits without sacrificing power, cost and data processing capacity (Sevenhans, 2000). An important goal in the design of ADCs is that of obtaining Spurious Free Dynamic Range (SFDR) of the order of 100 dB for signal bandwidth of the order of 30 MHz (Walden, 1999). The major challenge is that of designing and building low power wideband converters able to convert bandwidths of 10 ~ 30 MHz centered at RF frequency of 3 ~ 4 GHz while guaranteeing a resolution of 16 bit in order to satisfy dynamic range requirements of most transmission standards.

In order to avoid duplication of the receiver front-end hardware for each supported standard, the receiver front-end supporting multiple air interfaces have to be designed to process the widest channel bandwidth among the standards that have to be received. As an example, front-end receivers designed to support both DCS and UMTS, should be able to pickup signals over a 500 MHz band, extending from 1710 to 2170 MHz (in Europe). IS-95 requires a channel bandwidth of 1250 kHz, while UMTS channel bandwidth should be of the order of 5 MHz. The design of wideband receivers are hampered by a host of problems from power dissipation issues to proper operation in an environment with strong Adjacent Channel Interference (ACI) and Co-Channel Interference (CCI). For example, amplitude levels and frequency separations (the so called blocker offset frequencies  $\Delta f$ ) from the useful signal for GSM and DCS mobile and base stations are shown in Table I (GSM Rec., 1996). In the case of wideband receivers, designed to accept a composite signal such as those associated with FDM-based air interfaces,  $\Delta f < B_x$ , where  $B_x$  is the system front-end bandwidth that is dominated by the bandwidth of the Low Noise Amplifiers (LNAs) and filters. While for CDMA-based systems, a wideband receiver does not suffer from strong ACI (the interference is mainly co-channel and due to the other system users), for FDM-based air interfaces, such as GSM, the ADC in the analog chain has to cope with strong carriers of the channels adjacent to the useful signal. This problem requires ADC converters to be able to guarantee high dynamic range values

Table I. Blocker specifications for GSM and DCS (values refers to a desired carrier at +3 dB above the receiver sensitivity that is -100 dBm for DCS mobiles and -104 dBm for other radio types).

Blocker Offset $\Delta f$ [MHz]	DCS-MS [dBc]	DCS-BTS [dBc]	GSM-MS [dBc]	GSM-BTS [dBc]
0.6-0.8	+54	+66	+63	+75
0.8-1.6	+54	+76	+68	+85
1.6-3	+64	+76	+78	+85
>3	+71	+76	+78	+88

and adequate SNR specifications in order to permit the separation of a potentially weak desired signal from a strong ACI.

Practical problems by which receiver front-end have to cope with can be summarized as follows.

- Co-channel interference; it is usually specified by a threshold power level above which the desired signal power should lie. Typical CCI values fall in the range of 9-20 dB. In the GSM air interface for example, the required CCI protection must be greater than 9 dB.
- Adjacent channel interference; since the receiver front-end should be designed in order to receive the widest signal bandwidth associated with a multitude of communication protocols, interfering signal rejection which does not take place in the analog segment, should be conducted in the digital domain after the ADC.
- Image components; these are signals that are centered around frequencies whose distances from the mixer oscillator frequencies are equal to an integer multiple of the distance between the frequencies of the desired signal and the frequency of the Local Oscillator (LO). For instance in the case of a single mixing stage down to an Intermediate Frequency (IF), the nearest image frequency  $f_{IM}$  satisfies  $|f_{LO} - f_{IM}| = |f_{RF} - f_{LO}|$ . This scenario is pictorially shown in Fig.1. Image components are often attenuated by the RF filter placed before the first mixing stage.

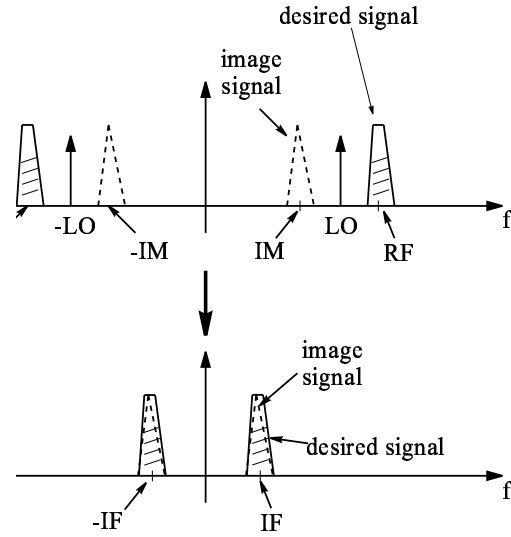


Figure 1. Image Spectra after first IF mixing.

## 2.1. RECEIVER FRONT-END TECHNOLOGY

The most common approaches to the design of the front-end can be summarized as follows:

1. First mixing stage using analog circuitry down to IF, followed by a second mixing at IF down to baseband followed by ADC conversion (i.e., the classic double heterodyne receiver).
2. First mixing stage using analog circuitry down to IF followed by ADC conversion at IF.
3. Zero IF or direct conversion design whereby there is a single mixing stage down to baseband (or quasi-baseband) followed by ADC conversion.
4. Direct ADC conversion of the wideband signal after the Low Noise Amplifier (LNA) stages which must implicitly perform the AGC function.

In what follows we provide an overview of the aforementioned approaches to the design of receiver front-ends, and explore the advantages and disadvantages of different approaches.

### 2.1.1. Double DownConversion Stage: The Heterodyne Approach

A classic narrowband receiver front-end contains both analog and digital stages, as shown in Fig. 2. In this architecture, analog to digital

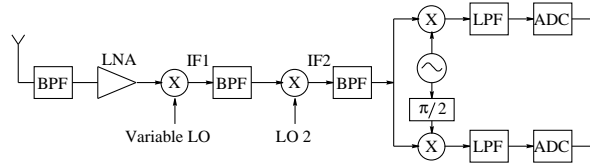


Figure 2. Super Heterodyne Front-End Architecture I.

conversion is performed at baseband after a double down conversion stage whose purpose is to shift the useful RF signal down to the baseband. Such an architecture is currently adopted in cellular base stations and hand held radio receivers. Due to its narrowband nature, it has the drawback of requiring replication of the same structure for every narrowband channel to be received via redesign of the analog components which are tuned to a specific channel.

In Fig. 2, the first BPF accomplishes the task of rejecting the out-of-band signal components (i.e., performing image reject) before the signal is passed on to the first mixing stage. Practically, IF mixing is handled in two stages in order to select the frequency band of interest related to a specific air interface. In particular, the first IF mixer is frequency tunable with a pre-specified stop-band mask, while the second has a fixed bandwidth. The frequency of the first mixer has to be changed so that the output signal falls in the input bandwidth of the second IF mixer. In the receiver architecture shown in Fig. 2, the received RF signal inputs a cascade of LNAs. The LNA accomplishes the task of amplifying the RF signal, which typically falls in the  $\mu V$  range, to within the dynamic range of the first mixer avoiding amplitude mismatch between the two mixer inputs, so that the signal at the end of the downconversion stages at the input of the ADC has sufficient amplitude that matches the input dynamic range of the ADC (the amplifier chain in the downconversion stages of a heterodyne receiver should typically supply an amplification on the order of 100 dB in order to compensate for signal attenuation due to propagation, mixing and filtering). A common drawback of the scheme is the fact that the LNA should drive a low impedance of typically  $50\text{-}\Omega$  (standard system design is based on a  $50\text{ }\Omega$  transmission chain) due to the analog image-reject filter. As we will outline below, this problem does not exist for the Zero-IF scheme since such filters are not needed. In Fig. 2, another filtering stage after LNA and before the first mixing stage is sometimes inserted to further attenuate image frequencies. A variable gain amplifier before second downconversion stage can be inserted to implement the Automatic Gain Control (AGC) function with the task of amplifying the IF

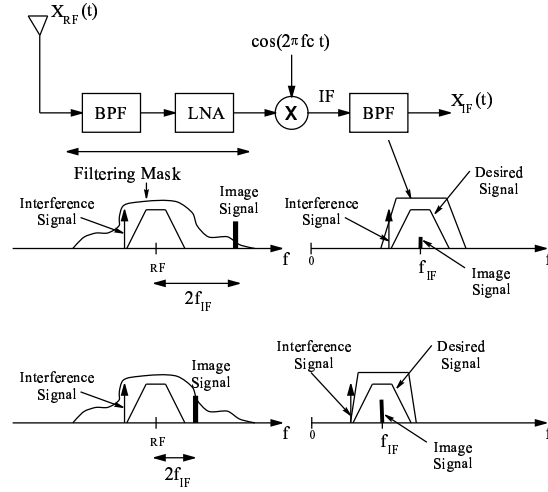


Figure 3. First Stage of a typical receiver Front-End.

signal in order for its amplitude to match the input dynamic range of the subsequent stages.

The advantages of this classic receiver front-end derive from the availability of low cost narrowband RF and IF analog components with low power consumption. However, one drawback is the fact that the main components of the design are based on fixed narrowband devices designed for a specific application.

Fig. 3 pictorially highlights the problems related to the choice of the IF frequency with respect to the filtering mask created by the BPF and the LNA amplifiers before the first mixing stage. Using filters with the same relative bandwidth as measured by the quality factor or Q values before the mixing stage, large values of  $f_{IF}$  lead to considerable image signal attenuation, but lets adjacent channel signals to pass through the filtering stages almost unattenuated. On the contrary with small values of  $f_{IF}$ , it is possible to obtain a better adjacent channel interference rejection, but worse image signal attenuation. In actual implementations, a set of discrete oscillators and surface-acoustic wave (SAW) filters are used to perform the main front-end mixing and filtering tasks for PCS applications. But these devices are generally not tunable.

After baseband ADC conversion, a channelizer accomplishes the task of isolating the desired channel while rejecting the adjacent channel interference in the case of a FDM based air interface, or despreading the composite signal in the case of a Direct Sequence (DS) CDMA based air interface. Other technical solutions, resembling the architecture

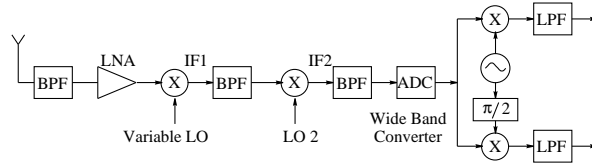


Figure 4. Super Heterodyne Front-End Architecture II.

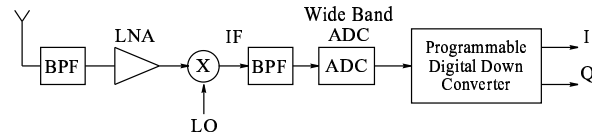


Figure 5. Single Down Conversion Front End Architecture.

depicted in Fig. 4, have been deployed with the goal of shifting the ADC as much as possible toward the antenna.

From a third and fourth generation perspective, the super heterodyne approach is not a good alternative because of its narrow and fixed band nature. Furthermore, imperfect phase splitting between the In-phase and Quadrature components due to gain and phase mismatch between the two branches, could lead to imperfect cancellation of the image components. Finally, this architecture does not allow full integration in a single Integrated Circuit (IC) chip because of the number of discrete components needed. The goal of IC designers is to integrate as many of the discrete components as possible in a single chip in order to avoid mismatch effects.

### 2.1.2. Digital Receivers: the Single Downconversion Approach

The receiver front-end could be designed in order to operate over a wider bandwidth with respect to the heterodyne solution, so that after first down conversion stage, specific channels could be isolated via channelizers.

The IF bandpass filter does not need to sharply cut-off out of band frequencies (sharp filtering is achieved by the channelizer often implemented digitally), making the front-end cheaper than the heterodyne approach. Major advantage of this technique relative to the heterodyne approach arises from the consideration that there is no need to duplicate the front-end when more than one channel should be received.

While the first down conversion stage is identical to that of the heterodyne receiver front-end, the BandPass Filter (BPF) before the ADC does not need to be narrowband because IF tuning and filtering is accomplished in digital fashion via a Programmable Digital Down Converter (DDC). From a practical point of view, the architecture under

Table II. Performance of the Digital Down Converter (DDC) from Harris Semiconductor, HSP50016.

Max Input Data Rate	Maximum Input Data Resolution	SFDR	Decimation factor	Passband Ripple	Stopband Attenuation
75MSPS	16-bit	102 dB	32-131072	<0.04 dB	>104dB

examination resembles the one shown in Fig. 5. Sampled data from the ADC are input to a digital downconverter, whose purpose is to a) shift digital sampled signal toward the baseband digitally, b) decimate the resulting signal down to the Nyquist rate (or slightly higher in practice) and c) digital filtering to isolate the useful baseband signal. Precise signal tuning is accomplished through Numerically Controlled Oscillators (NCOs), able to down-convert a sampled signal with minimal gain and phase imbalance between the in-phase and quadrature components.

Sample practical DDC performance metrics are shown in Table II for the DDC HSP50016 from Harris Semiconductor.

### 2.1.3. *WideBand Receivers: Zero-IF Architecture*

Zero-IF receiver front-end is shown in Fig. 6 and is specially suitable for user terminals because of the low power dissipation and the low cost associated with the reduced number of components which in turn, guarantees a higher level of integration than the previous architectures.

This scheme does not suffer from the problem of image signal as in the case of receivers with down conversion to IF since effectively the IF frequency is zero. Gain mismatches and phase errors could lead to moderate SNR losses. Since zero-IF design does not have the problem of image signals, the pre-selection RF filter could be avoided. However, in practice, it is still needed to reject out-of-band interfering signals that could create distortion due to the intermodulation products generated after the mixer.

Lowpass filters have the task of isolating the desired baseband signals. Other analog circuits appear in the baseband section of the in-phase and quadrature branches and hence consume less power. Precise phase matching is necessary in order to avoid the negative part of the signal spectrum to alias the positive part of the spectrum after down conversion to baseband.

The Zero-IF design imposes some constraints on the analog components of the front-end, but it is a more hardware efficient architecture.

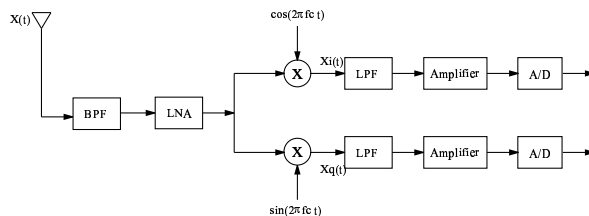


Figure 6. Zero-IF Receiver Front-End.

In such a design the analog components must have very high dynamic range and high sensitivity. These constraints make it difficult to find commercial components that meet the specifications, and in any case such components tend to be very expensive even if found. In particular, a direct conversion front-end requires high-gain low-noise mixers, very precise I and Q phase balancing of the quadrature demodulator, highly-selective filters and provisions for DC offset cancellation.

Some of the key problems of the zero-IF architecture may be summarized as follows:

- LO leakage: this problem derives from the fact that the local oscillator used for downconverting the RF signal produces a signal at the central frequency of the bandpass filter and the low noise amplifier after the antenna. Because of the imperfect mixer isolation, possibly due to capacitive substrate coupling or due to the bond wire coupling in case the LO signal is externally connected to the mixer, a fraction of the LO signal energy goes back into the RF port of the receiver and arrives at the antenna and is subsequently radiated as a signal at the same RF frequency. This signal could act as an inband interference with respect to other portable receivers tuned to the same frequency, worst yet, it is re-received by the same receiver creating interference with the useful signal. This problem is less evident in super heterodyne architectures because the first LO oscillator produces a signal whose frequency does not lie in the RF antenna bandwidth. Although this problem still exists for heterodyne architecture, its effects on the analog segment are eliminated by the IF filtering section.
- DC offset: this is primarily due to mismatch between the transistors in the signal path from the mixers to the filtering stages and to the I&Q components until the detector. However, there could be interfering signals, such as the same signal coming from the LO leakage which is again self mixed down to baseband as a DC component, or near-band channels that pass unfiltered after the first RF bandpass filter and are mixed to baseband by the mixers.

The main problem related to these kinds of interfering signals is that they are frequency dependent and their magnitudes vary as a function of the position of the mobile terminal (Abidi et al., 1995). Since offset appears centered around DC it cannot be filtered by capacitive coupling because then the useful signal would be cut off as well. A notch analog filter with a very small bandwidth, say around 5 Hz, could be used to cut off the DC components, while paying attention to limit the loss of the useful signal. For example, Abidi (Abidi et al., 1995) estimated that for GSM-like receivers, in order to obtain a BER of  $10^{-3}$  with a signal bandwidth of 200 kHz, a notch filter with a 5 Hz bandwidth around DC, causes a loss in the receiver sensitivity of about 0.2 dB. Under the same conditions, the receivers did not function with the target BER when the notch filter bandwidth reached 20 Hz. A possible way to remove the DC offsets consists in digitally evaluating the long term mean value of the samples at the ADC output. With this method, a window of data is collected periodically, its mean value is calculated and converted into an analog signal using a DAC, that is then subtracted from the analog baseband signal output from the mixers. This approach has been used by Alcatel (Haspeslagh et al., 1992) in their proposed GSM receivers. Samples of the baseband signal are averaged in a 8-bit format using a DSP over a sampling window that could be programmed. Offset correction takes place before baseband ADC conversion as shown in Fig. 7.

Another offset correction scheme has been proposed in (Tsurumi et al., 1999). It differs from the one proposed in (Haspeslagh et al., 1992) because offset correction is conducted after ADC conversion. This double scheme correction is used because in the case a low level signal is received, only a digital correction could be sufficient for satisfying system requirements. However, as proposed by (Haspeslagh et al., 1992), correction before ADC is useful in the case large signals are received in order to avoid input AD saturation. Doing so, the offset compensator placed before ADC has the task of counteracting the time invariant offset, while the digital compensator accomplishes the task of decreasing the time variant DC offset. In their system, this combined method was able to guarantee only a  $\frac{E_b}{N_o}$  degradation of about 0.4 dB at a BER of  $10^{-2}$  and with a DC offset equal to 25% of the ADC full scale.

- $\frac{1}{f}$  Noise: the flicker noise is a phenomenon that occurs in semiconductor devices and has a power spectral density that is inversely proportional to the frequency. It is produced by phenomenon with a certain degree of physical memory and it is mainly due to the

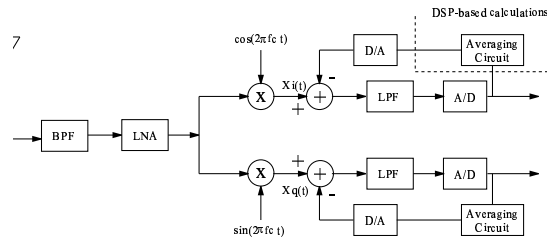


Figure 7. Offset correction proposed by Haspeslagh.

non-reversible variation of the characteristics of semiconductor devices. Flicker noise affects received signal mainly after downconversion to baseband. In particular, since the signal level is of the order of  $100\mu V$  at the antenna, flicker noise represents a substantial fraction of the total signal power, causing distortion of the received baseband signal. Flicker noise power spectral density level intersects the thermal noise floor generally at frequencies of several MHz and is dependent on the process technology used for IC fabrication. In the Zero-IF scheme, the noise floor is amplified in the RF stages and hence, the frequency intersection point referred to above is consequently lowered. In a recent paper (Namgoong et al., 2001), the authors estimated that in the case of a RF section amplifying the signal by 25 dB and having a noise figure equal to 5 dB, noise floor increases by 30 dB with respect to the thermal noise and subsequently, the flicker noise intersection frequency reduces to several kHz. These analysis are useful to the system designer in that they determine what kind of noise levels the designer has to deal with. Finally, concerning the superheterodyne receivers, we should say that since the signal is mainly amplified during the IF stages,  $\frac{1}{f}$  noise becomes insignificant at baseband when compared to the received signal amplitudes at that stage. Further details about the effects of this noise in Zero-IF receivers can be found in (Namgoong et al., 2001).

- Inter-Modulation Distortion (IMD): intermodulation distortion represents a significant problem particularly in PCS applications. InterModulation (IM) products produce distortion of the desired baseband signal. Particularly problematic in Zero-IF receivers, IM products are produced by non ideal mixers. In order to compensate for their effects, the receiver specifications for dynamic range should be modified. For example, (Tsurumi et al., 1999) has indicated that the required value of margin on useful signal level relative to the distortion level should be 15 dB. This requirement

adds to the dynamic range of the receiver calculated by considering the blocking signal specifications required for the specific air interface, leading to even more stringent requirements for the ADC converters used in the front-end. In a recent paper (Tsurumi et al., 1999), the authors proposed an IM distortion correction system which generates a feedback control signal acting on the mixers by changing their bias current. This control signal is generated in the digital stage with the goal of achieving a predefined BER specification of the proposed system.

One of the critical components of a Zero-IF receiver is the local oscillator that should produce a frequency equal to the RF frequency at which the received signal is centered. The problem is to generate accurate quadrature sinusoids with acceptable amplitudes to down convert the received signal to baseband. This problem becomes more and more challenging as the frequency is increased. Practically, quadrature signals are often produced using a single sinusoidal signal generator tuned by an LC circuit, and a phase-shift circuit. Phase-shift imperfections of the order of  $1^\circ$  are often required in practice.

## 2.2. ADC DESIGN IS STILL THE KEY CHALLENGING PROBLEM FOR BROADBAND SR SYSTEMS

Wideband converters used in SR applications, are exposed to a large number of carriers coming from different sources. In mobile applications, in presence of shadowing and fading and imperfect power control, the different carriers defining the composite wideband signal experience widely varying attenuation levels. In what follows, we summarize the major requirements imposed by such transmission conditions on the ADC converters.

### 2.2.1. *Blocking Signals*

In a wideband receiver, the received carriers are often characterized as having a dramatic difference in their RF power levels. It is this difference that affects the performance requirements of the wideband ADC converters. As an example, consider the practical case in which two carriers are received by a wideband ADC converter, and let us suppose one carrier as blocking (by virtue of its enormously larger power level) and the other as wanted. Moreover, let us assume that  $P_B$  is the power of the blocking signal and  $P_W$  is the power of the desired signal such that  $P_B \gg P_W$ . For instance, in order to comply with GSM specifications, the receiver should be able to distinguish a blocking signal with power up to about 85 dB over the useful signal power (i.e.,  $P_B \leq P_W + 85 \text{ dB}$ , where the two signals are 0.8 MHz to

1.6 MHz apart, or 8 GSM channels (JSAC, 1999)). The Spurious Free Dynamic Range (SFDR) is an important performance measure used in wide-band receivers. It indicates the capacity of the ADC to accurately detect a low-level signal in an environment with strong interference. A receiver front-end with a specified SFDR value is capable of detecting both a weak and a strong signal whose power levels differ by no more than the specified SFDR. In particular, SFDR is the ratio between the desired sinusoidal signal power to the peak power of the largest spurious signal in the output spectrum of the ADC converter. Note that SFDR is different from the Signal to Noise Ratio (SNR) because it takes into account the non-linearity effects and it is an additive term that adds to the minimum SNR required for the wanted signal which is dictated by other system requirements such as the minimum acceptable Bit-Error-Rate (BER). Spurious signals are generated as a result of quantization and non linearities in the input stages of the ADC, such as in the sample and hold circuits. The required minimum value of SFDR needed could be expressed as:

$$SFDR_{min} = 10 \log\left(\frac{P_B}{P_X}\right) + SNR_{min} \quad (1)$$

For the GSM example noted above, the power ratio between blocking and wanted signal results in an increment in ADC resolution with a number of bits equal to about 14 bit. This increment in the ADC resolution represents the protection the ADC needs to provide against blocking signals.

Average currently practical values of SFDR and bandwidth for various air interfaces is about 80 dB and 5-20 MHz respectively.  $SNR_{min}$  values depend on the specific transmission system. For example, GSM and DECT require  $SNR_{min}$  on the order of 10dB, while GPS system requires  $SNR_{min} \propto 6 - 12$ dB.

### 2.2.2. Interference Due to Near Critical Sampling

Sampling the signal at the Nyquist frequency could lead to some practical problems. First, the distortion due to the analog filters before the ADC converter may affect the signal samples after the ADC converter. Second, there is the problem of the image signal; namely, interference signals centered around frequencies that after downconversion to an intermediate frequency, may fall within the bandwidth of the filter placed after the first mixer (see Fig. 3).

Sampling the signal at Nyquist frequency translates an undesirable signal at a frequency that is 1.5 times the sampling frequency, into the desired signal band. This situation is shown in Fig. 8 where the desired signal has bandwidth limited to the frequencies  $[-\frac{B}{2}; \frac{B}{2}]$ . Since

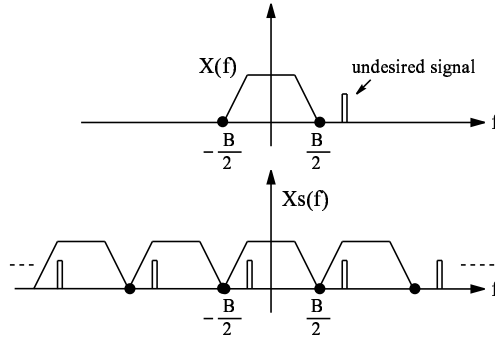


Figure 8. Overlap of the undesired signals into the useful band due to critical sampling.

in the transform domain sampling generates replicas of the desired signal spectrum over a specified band, the undesired signal translates to baseband where the useful signal lies causing aliasing.

A practical approach to remedy this problem consists in limiting the distortion due to the undesired signal relative to the distortion caused by the ADC non-linearities in the spectrum of the signal at the output of the ADC. Oversampling could obviously reduce the effect of large interfering signals close in frequency to the Nyquist bandwidth of the desired signal.

The adjacent channel interference specifications depend on the multiple access scheme adopted for the desired air interface. While in CDMA based standards there is no adjacent channel interference because all coded signals cover the same bandwidth (there is however significant cochannel interference present), in FDMA based air interfaces any useful channel has several adjacent channels. In the latter case, the receiver has to be able to detect the desired signal from a bandwidth containing many interfering signals, in compliance with the SFDR requirements for the system. As an example, the GSM standard specifies a mask showing the power level of the adjacent interfering signals which ensures that desired channel could be detected from a wideband signal with acceptable fidelity level.

### 3. Architecture of the Prototype Test Platform

This section outlines the development of a PC-based prototype software radio system designed and build utilizing a powerful front-end technology that is explored in a further section. The SR receiver is based on a 800 MHz Pentium III processors. The operating system adopted

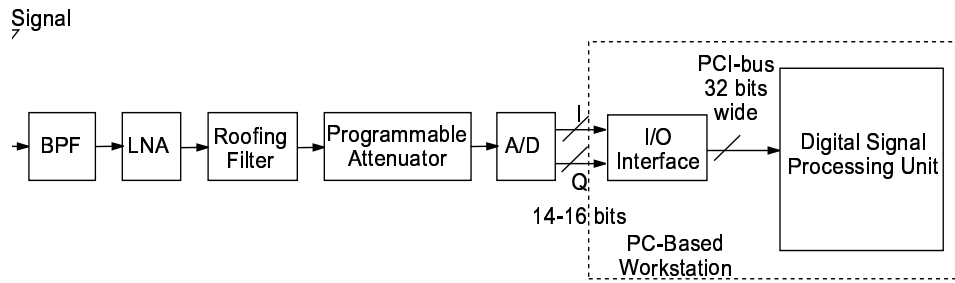


Figure 9. Receiver architecture.

for the workstations has been the Linux operating system because it guarantees the maximum accessibility to all the computer resources, such as device drivers for Input/Output (I/O) operations, and because it is shareware.

For the design presented in this paper, no kernel tuning has been performed to prioritize processes, although the workstations have been primarily used to run the software transceiver code. The system has a 33 MHz PCI bus which is 32 bits wide. The receiver functionalities have been implemented in software using a high level programming language. This design approach allows the transmission parameters to be reconfigured in a simple manner. The software radio prototype has been conceived to support real-time AMPS and GMSK transmission and reception.

The high-level receiver architecture for both reception systems is shown in Fig. 9. It is composed of two main blocks, an analog radio subsystem and a signal processing subsystem which communicates with the front-end through an I/O interface. The receiver analog front-end is based on a wide-band delta-sigma ( $\Delta\Sigma$ ) converter which converts a useful signal with RF bandwidth up to 100 MHz centered around a RF frequency up to 2 GHz from the antenna in a sampled data stream down to baseband (i.e., direct conversion or zero IF design). The output of this ADC converter subsequently feeds the workstation via an I/O interface card. This latter functionality will be discussed later, but its main function is to absorb processing jitters due to operation in a general time-shared workstation.

### 3.1. THE PROGRAMMING ENVIRONMENT

In order to specify the physical layer of the transceiver structure, a programming environment has been developed. The environment allows real time processing of the samples of the signal in a time driven sample-

by-sample or block-by-block fashion. The environment consists of a simple programming language with semantics allowing direct definition of the system structure, a library of processing blocks and a general management program.

The management program controls the signal flow, while the actual processing is performed by a sequence of processing blocks belonging to the environment library. In the management program, system parameters such as the sampling rate, the bit rate and number of samples per symbol (in case of digital transmission) are defined, and the control variables of various blocks are updated. The processing blocks may operate with samples of the complex envelope of the narrowband signals, or with real samples of baseband or quasi-baseband signals.

For the demonstrator described in this paper, two different reception schemes have been considered, demonstrating the possibility of processing both AMPS and GSM-like signals. The specific processing architecture of these two systems are described in the following.

### 3.1.1. *Simulated AMPS Receiver System*

The system allows continuous transmission of an FM modulated signal containing both an analog component (the voice signal) and a digital component (a data signal containing all the signaling information). The voice signal, either acquired through an external acquisition system or synthetically generated, is added to the Manchester modulated data signal with bit rate of 9 Kbit/s. The resulting signal is then frequency modulated and transmitted. The modulated signal has RF bandwidth equal to 30 KHz.

The software processing includes a hard limiter, band-pass filter and frequency demodulator. The voice signal is recovered by lowpass filtering of the demodulated signal, while the data signal is recovered after matched filtering and sampling. The sampling signal is generated by an IF rectifier clock recovery subsystem, composed of an envelope detector, tuned resonator and timing generator. Four different frequency demodulation techniques have been implemented, namely (1) direct evaluation of the instantaneous frequency; (2) PLL based frequency demodulation; (3) differentiator followed by amplitude demodulation; and (4) correlation receiver. The four structures achieve very similar processing speeds and signal-to-noise ratio performances. Maximum, minimum and average processing speed in samples per second of the AMPS receiver are reported in Table III.

Referring to Fig. 9, the wideband ADC converter front-end outputs two sample streams at a constant rate, one for the in-phase component and the other for the quadrature component of the signal around the carrier (i.e., samples of the complex envelope of the information bearing

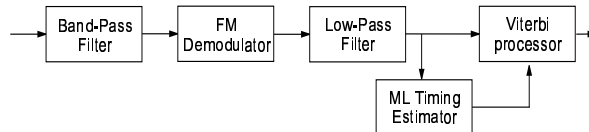


Figure 10. Block diagrams of the GSM-like receiver implemented in software.

baseband signal). The I and Q samples each have a resolution of 14 bits. The ADC converter has an embedded down-conversion system which outputs the samples of the input signal directly in baseband. This approach has the advantage of avoiding the need for rate conversion filters in the succeeding signal processing units.

Subsequently, the I/O interface captures the I and Q samples, collecting them in a block of 32 bit words. The functionality necessary for performing data transfers is embedded in the I/O board. The collected data is subsequently divided into their in-phase and quadrature components via software, through logic operations such as logical AND and Shift acting on bits.

The data, grouped in blocks of 32 bit samples by the I/O interface, are transferred to the processor through the 32 bit PCI-bus using the Direct Memory Access (DMA) transfer mode. In this manner, while the digital signal processing routines are processing the AMPS data stream of the previous data block, a new block of data is transferred to the user space. Note that the signal processing operations are strictly related to I/O, so that the former always has a block of sampled data to process. This approach guarantees the use of the whole PCI bus.

### 3.1.2. Simulated GSM-like System

In the simulated GSM-like system, the attention has been focused on the reception of a binary GMSK modulated signal. The receiver architecture is depicted in Fig. 10. The software processing includes a band-pass filter, a frequency demodulator, a low-pass filter and a sampler. The sampling signal is generated by a Maximum Likelihood timing estimator. The receiver uses 5 samples per symbol and therefore runs at a speed larger or equal to  $203 \times 5 = 1015$  Ksamples/s. Maximum, minimum and average processing speed in samples per second of the GSM-like receiver are reported in Table III.

All the I/O data transfers are performed in a manner similar to that of the AMPS demonstrator.

Table III. Processing speeds in Ksamples/s for the simulated AMPS and GSM-like systems.

Speed [Ksamples/s]	Average	Maximum	Minimum
GSM-like Receiver	1200	1300	1050
AMPS Receiver	1700	1800	1200

### 3.2. THE FRONT-END

The transceiver front-end is powered by delta-sigma ( $\Delta\Sigma$ ) data converter technology that is capable of operating at speeds in excess of 2 GHz. The process of frequency translation is built into the architecture of the ADC and DAC converters. Initial prototype chips have been fabricated using 0.6  $\mu\text{m}$  GaAs MESFET technology from Vitesse Semiconductor, Inc. Additional chips have been developed using SiGe technology, which has the advantage of being able to be fabricated on the same silicon substrate as conventional CMOS VLSI circuits.

#### 3.2.1. Overall Structure

The block diagram of the software radio front-end showing the critical components is shown in Fig. 11. The use of multiple antennas at the transceiver front-end is more a technological requirement than a system constraint. Generally speaking, antennas and tuned circuits at the front-end are efficient constant  $Q$  elements ( $Q$  is the quality factor of the tuned resonator). Using present technology, it is very difficult to construct a single antenna element and efficiently couple the received power to the Low-Noise-Amplifiers (LNAs) and transmit power from the Power-Amplifiers (PAs) to the antenna over a frequency band ranging several decades. Same argument holds for the design of LNAs and Power-Amplifiers. Hence, from a practical point of view it is essential to have multiple antennas and corresponding analog front-end elements to efficiently receive and transmit signals over a band of frequencies spanning several decades.

In the block diagram of Fig. 11, we show high speed Transmit/Receive (T/R) switches. This is not meant to be restrictive in any sense and

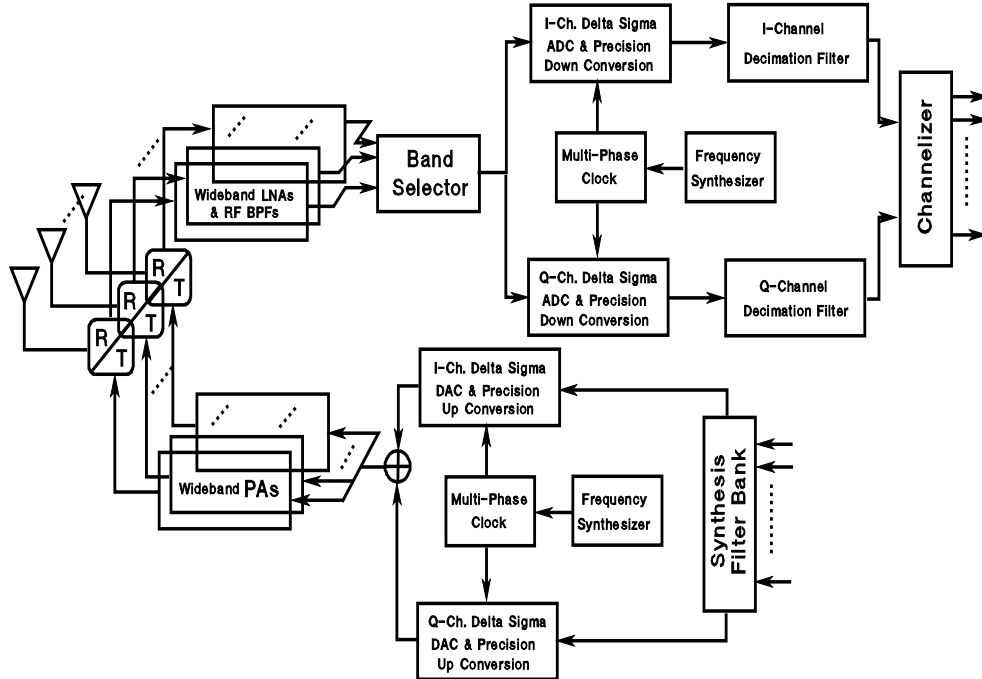


Figure 11. The global architecture of the front-end.

diplexers could easily be accommodated in the structure. As a matter of practice, efficient means of coupling signal power to the antenna and receiving power from the antenna is only possible if there is sufficient isolation between the transmit and receive ports. This is typically done by either switching between transmit and receive modes, or using simultaneous transmission and reception on two different frequency bands with sufficient separation, using a diplexer. Obviously, we may also employ a combination of the two techniques. Other potentially useful elements such as roofing filters and Automatic Gain Control (AGC) amplifiers are not shown for simplicity.

In the receive path of Fig. 11 we show a band selector which essentially switches among the multiple frequency bands allocated by FCC for different applications. The analog to digital conversion beyond this point is performed using the proprietary high-speed ADC from TechnoConcepts, Inc. ([www.technoconcepts.com](http://www.technoconcepts.com)) that performs precision down-conversion of the signal. The signal processing after band selection may be described as follows:

- the In-phase and Quadrature (I&Q) paths are distinct and are clocked by very precise in-phase and quadrature clock signals. The

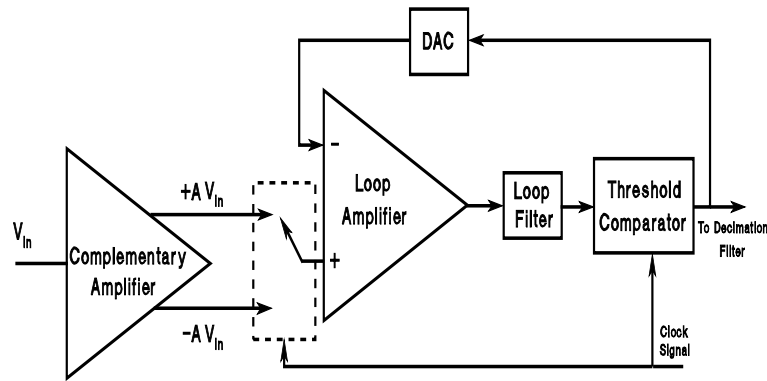


Figure 12. Block diagram of the  $\Delta\Sigma$  A/D converter.

clock signals themselves are generated from a frequency synthesizer that generates a signal at twice the center frequency of the band being digitized. A precise phase splitter generating the desired I&Q clock signals follows the frequency synthesizer;

- the bandwidth of the ADC converter is very large and usually several frequency channels associated with a given standard are digitized in one shot. In order to separate out distinct frequency channels, a channelizer which could be in the form of an analysis filter-bank is used to generate complex data streams corresponding to the samples of the complex envelopes of the signals in different frequency bands. Resampling, rescaling, and phase correction of the digitized waveforms can either be performed on the composite signal just prior to the channelizer, or on individual channels after the channelizer;
- the combined precision down-conversion using a single master clock and subsequent channelization, resampling, rescaling, and phase correction operations essentially allow the front-end to pick up signals associated with different air-interfaces. The oversampling factor of the signal is application dependent but at the very minimum, 5 samples per symbol are generated and subsequently processed;
- channel selection operations and further signal processing is performed after the channelizer but is not shown in the figure for simplicity.

The transmit side of Fig. 11 essentially performs the inverse operation as that of the receive side. Inclusion of the frequency synthesizer and multi-phase clock generator in the transmit block diagram allows for

possible simultaneous operation of the unit in both transmit and receive modes possibly over two distinct frequency bands and possibly using different antennas.

### 3.2.2. $\Delta\Sigma$ converter architecture

The high speed delta-sigma ( $\Delta\Sigma$ ) modulator A/D with embedded precision down-conversion is a classic design with several modifications and integration of critical functions on a single substrate to achieve significant performance improvements over traditional designs. The block diagram of the  $\Delta\Sigma$  modulator is shown in Fig. 12. The main features of the design are:

- the complementary amplifier provides a negatively and positively amplified versions of the input signal to the switching port. Precision down-conversion is essentially achieved by commutation and subsequent filtering in the rest of the modulator;
- the ADC resolution is determined by the oversampling factor and the loop filter order. More precisely, 1.5, 2.5, 3.5, and 4.5 bits of resolution per octave oversampling ratio is achievable for loop filters from first to fourth order. The commutation frequency is the same as the center frequency of the band that is to be down-converted to near DC and digitized. As an example, for a second order loop, at a center frequency of 1 GHz, and for a RF bandwidth of 10 MHz around the center frequency, the oversampling ratio is 100 or 6.6 octaves. The resulting resolution is greater than 16 bits resulting in about 99 dB of raw dynamic range. Down-conversion via commutation greatly enhances the dynamic range and allows for precise control over the clocking phase of the in-phase and quadrature components;
- down-conversion of the signal to a frequency near DC but not to DC allows for utilization of digital filters to eliminate DC offset effects of the analog components in down stream signal processing stages;
- the loop filter is based on simple analog designs greatly enhancing the ADC bandwidth and completely eliminating the need for Switched Capacitor Filters (SCF). The problem of SCF is that they cause aliasing and hence interference. Eliminating the SCF, the ADC can use continuous time filter with lower order and allows operation of the loop at much higher frequencies;

- the ADC uses commutation for down-conversion of the RF signal as opposed to sub-sampling which requires tremendous precision and femto-second pulses to achieve high resolution;
- all the components of the ADC converter are integrated on a single substrate using novel circuit solutions completely avoiding the need to exit the IC reducing costs, size, and eliminating the problem with circuit non-idealities;
- a novel super-linear commutating amplifier is used at the input stage as the core of the design;
- the overall design uses a current steering technique based on Gallium-Arsenide MESFETs and Silicon-Germanium devices resulting in constant power dissipation regardless of the center frequency of the signal to be down-converted and digitized.

The architecture of the Digital to Analog Converter (DAC) is much the same as a classic  $\Delta\Sigma$  demodulator but switching via logic gates is used for up-conversion of the baseband signal to around the carrier frequency.

### 3.3. THE I/O INTERFACE

The main problem that arises using a workstation as the software radio platform concerns the rate at which transceiver operations are to be performed. For real-time operation, the data flux from the ADC with embedded precision down-conversion, and to the DAC with embedded precision up-conversion is constant. However, as noted earlier, since the transceiver operation is run in software and is under the control of the Linux kernel, the rate at which data is processed by the workstation is not constant. In order to avoid any kind of jitter due to rate fluctuations for task scheduling and memory management operations, an I/O interface board has been used. This board is a PCI form factor ultra high-speed digital I/O card and consists of 32 bit digital input and output channels. Due to the high rate by which it executes data transfers, this board is particularly suited for high-speed digital I/O applications. It performs the data transfer using bus mastering DMA via a 32 bit PCI bus architecture. The maximum data transfer rate is 80 MHz. Use of DMA transfer mode allows the main processor load to be reduced, since the data transfer takes place in background, while the main processor performs digital signal processing on the previous input data stream. The use of an I/O board has the effect of eliminating the need for any kind of timing synchronization between the analog front-end and the main processor. The I/O board decouples the

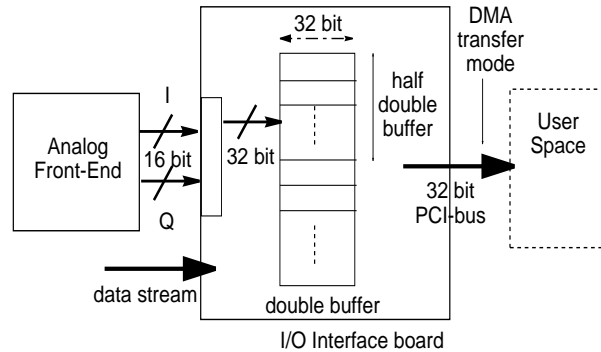


Figure 13. Block diagram of the I/O system for the receiver side.

instantaneous rate by which the analog front-end produces data from the rate by which the previous block of data are processed by the CPU.

The board has a set of C-language routines that makes all data transfer management operations simple. The architecture of the I/O system for the receiver side is shown in Fig. 13. A similar structure is used for the transmitter side of the transceiver. The only difference concerns the direction of data flow.

The data transfer occurs at the ADC word sample rate (since the architecture of the ADC is that of delta-sigma, the raw sample rate is much larger than the word rate at the output) by using the external clock mode. This operational mode is mastered by the clock source coming from the ADC converter. In particular, it is the same clock used by the ADC after the decimation filtering of the signal. The I/O board samples a 32 bit input word on the positive edge of the clock. In this manner it is guaranteed that I/O board samples a valid data from the ADC converter.

The continuous data transfer in real-time mode is guaranteed by the double-buffered asynchronous continuous digital input programming scheme. The principle behind this operation mode is to use a circular buffer logically divided into two equal halves. The buffer length is set before every input transfer starts in order to guarantee real-time operation. Before the effective receiving phase begins, the I/O board is set to support digital input operations in an asynchronous mode. The term asynchronous refers to the fact that the data transfer takes place only after a certain amount of data has been transferred to the input board from the receiver front-end.

### 3.3.1. Determination of the circular buffer size

The key factor behind the determination of the buffer size concerns the need of guaranteeing real time transmission with acceptable delays. The operation rate is chosen so that the digital signal processing execution time in the workstation matches the time by which the I/O device board fills half of the circular buffer (it is also possible to transfer data at a rate less than the capacity of the digital signal processing stage). This condition is a system level constraint and assures that the signal processing routines always have correct samples to process. In other words, the condition assures that the Input data transfer is not a bottleneck for the overall system. As an example, considering the AMPS receiver, we may calculate that an input signal of useful bandwidth equal to 30 kHz produces an input data rate of about  $75 \frac{ksample}{s}$  if the oversampling factor is equal to 5 samples for input signal period and if the input signal is translated to baseband before being sampled by the front-end. This rate corresponds to a throughput of about  $r = 13.3 \frac{\mu s}{sample}$ , while the digital signal processing execution time is equal to  $0.58 \frac{\mu s}{sample}$ . This means that the platform is capable of correctly processing one AMPS channel.

In Fig. 14, the solid curve depicts the average time to transfer data from the receiver front-end to the user space, while the dotted curve reflects the average time required to process the data with the AMPS receiver, which is a constant value, plus the time to transfer data to the speaker. The average transfer times for both curves has been evaluated as a function of the buffer size, by averaging over one hundred transfers. From this figure, it is possible to observe that the time to transfer data is a decreasing function of the buffer size. This is due to the fact that a certain amount of time for transferring data is independent (within certain limits) of the total number of data samples transferred. Hence, increasing the buffer size, the overhead time associated with the intrinsic time for data transfer with the I/O board is reduced for each transferred sample. The dotted curve is increasing slowly because the time to transfer processed data to the speaker increases when more data are transferred. However, this latter time is much smaller than the average time used for data transfer from the input boundary to the user space. Of course, the drawback of using larger sized buffers is the overall system latency which must be within tolerable limits.

The time spent for transferring the data processed by the software routines, to the audio board falls in the range of  $[0.1175 \frac{\mu s}{sample}; 0.175 \frac{\mu s}{sample}]$  for buffer size in the range of [2000; 20000] samples.

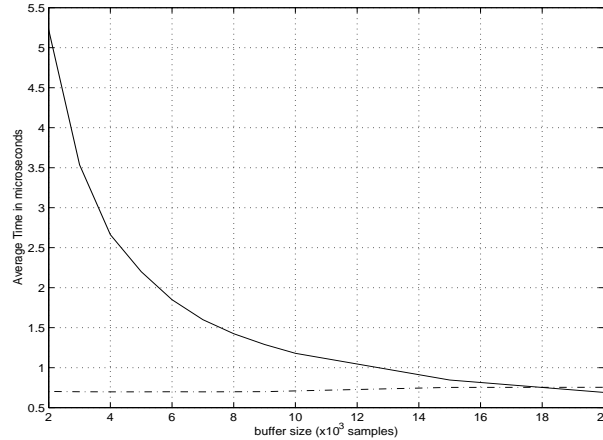


Figure 14. Average times.

In order to guarantee real time operation, the following equation, valid for both AMPS and GMSK receivers, must be met:

$$t_{proc} + t_{speaker} \geq t_{DI} \quad (2)$$

$$t_{proc} + t_{speaker} \leq r \quad (3)$$

where,  $t_{proc}$  is the average time spent by the software routines for processing an input sample,  $t_{speaker}$  is the average time spent for transferring a processed data sample from the user space to the audio board,  $t_{DI}$  is the average time spent to transfer half of the double buffer from the input boundary to the user space. Finally,  $r$  is the throughput explained at the beginning of this section. All specifications of time have been normalized with respect to the buffer size. For the AMPS receiver, this average time is about  $0.58 \frac{\mu s}{sample}$ , no matter what the buffer size. This value has been obtained by performing signal processing on 100 input data blocks. Note that, if Eq. 3 is not satisfied, the system may drop the data incoming from the front-end or may change the rate by which the processed samples are transferred to the audio board.

In the case of the AMPS receiver, taking into account the data shown in Fig. 14 and the time for data transfer to the speaker, a minimum buffer size of 18000 samples is needed in order to comply with Eq. 2. This value is actually half of the size of the circular buffer. Choosing a greater buffer size, it is possible to reduce the overhead time due to the call to the software routines, but at a price of increased latency.

An analogous discussion holds valid for the GMSK receiver. The only difference is that in this case, the processing time for each sample changes while all other timing constraints remain the same. All time

evaluations have been made by using the C-shell time (Turletti et al., 1999), which guarantees that the whole CPU is used for the application under examination.

#### 4. Conclusion

In this paper we have attempted to draw a potential evolutionary path for the transceiver architectures based on the SR technology that may be employed in the future broadband satellite communication systems. There are ample economic and practical reasons for such an evolutionary path to come to fruition. Subsequently, we have focused on the architecture of the transceiver front-end that still remains the key technological bottleneck to the proliferation of SR transceivers for both the space and terrestrial applications. Various architectures for digital receivers have been presented along with analysis of limitations and advantages of each scheme. Finally, we have presented the architecture of a prototype SR receiver we have designed, build and tested using a novel front-end technology based on a promising architecture that combines frequency translation and sampling. High level details of the ADC that is at the core of our design has been presented along with sample processing rates we have been able to achieve for AMPS like and GSM like signals.

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